WHAT IS CLAIMED IS:

1. A system-on-a-chip comprising:

a microprocessor;

a non-volatile imperfect semiconductor memory device;

a memory controller configured to transfer device data between the microprocessor and the non-volatile semiconductor imperfect memory device.

2. The system-on-a-chip of claim 1, further comprising:

a translator configured to translate logical block addresses to corresponding physical block addresses on the non-volatile imperfect semiconductor memory device during execution of a read or write command.

3. The system-on-a-chip of claim 1, further comprising:

error correction of data transferred between the microprocessor and the non-volatile imperfect semiconductor memory device.

4. The system-on-a-chip of claim 3, wherein the memory controller is configured to provide error correction.

5. The system-on-a-chip of claim 1, wherein the non-volatile semiconductor-based imperfect memory device is an atomic resolution memory device.

6. The system-on-a-chip of claim 1, wherein the non-volatile semiconductor-based imperfect memory device is a magnetic random access memory device.

7. The system-on-a-chip of claim 1, wherein the non-volatile semiconductor-based imperfect memory device is external to the system-on-a-chip.

8. A system-on-a-chip comprising:

a microprocessor;

a non-volatile semiconductor-based imperfect memory device; and

a memory controller configured to receive at least one data block from the microprocessor using an associated logical block address, to translate the associated logical block address to a corresponding physical block address, to provide for the at least one data block an error correction code that is a function of the at least one data block, to send the at least one data block and error correction code to the non-volatile semiconductor-based imperfect memory device using the physical block address, and to provide error detection and correction for the at least one data block based on the at least one data block and error correction code read from the non-volatile semiconductor-based imperfect memory device.

9. The system-on-a-chip of claim 8, wherein the memory controller further comprises:

a buffer memory configured to receive a plurality of data blocks, including the at least one data block, from the microprocessor and to send the plurality of data blocks to the non-volatile semiconductor-based imperfect memory device; and

a buffer manager comprising:

a hardware-implemented logic block configured to manage the transfer of the plurality of data blocks between the microprocessor and the non-volatile semiconductor-based imperfect memory device, wherein the buffer manager enables the microprocessor to access a first data block at a first location within the buffer memory while a second data block is concurrently being written to the non-volatile semiconductor-based imperfect memory device from a second location within the buffer memory; and

a memory mapping block configured to receive from the non-volatile semiconductor-based imperfect memory device a memory map

indicating reserved memory locations within the non-volatile semiconductor-based imperfect and comprising:

a hardware-implemented logic block configured to translate a logical block address to a corresponding physical block address based upon the memory map.

10. The system-on-a-chip of claim 9, wherein the buffer memory is configured as a circular buffer.

11. The system-on-a-chip of claim 9, wherein the buffer memory comprises a number of bit positions wherein the number of bit positions is a multiple of a number of bit positions in the at least one data block.

12. The system-on-a-chip of claim 11, wherein the number of buffer memory bit positions is a multiple of 512.

13. The system-on-a-chip of claim 9, wherein the buffer manager is further configured to receive from the microprocessor a plurality of set-up information blocks, wherein each of set-up information block comprises information to enable transfer of the plurality of data blocks between the microprocessor and the non-volatile semiconductor-based imperfect memory device.

14. The system-on-a-chip of claim 13, wherein each set-up information blocks contains information comprising a number of data block to be transferred and their associated logical block addresses.

15. The system-on-a-chip of claim 13, wherein the plurality of set-up information blocks is stored in a plurality of set-up registers.

16. The system-on-a-chip of claim 15, wherein the memory controller further comprises:

a processor translator comprising:

a hardware-implemented logic block configured to synchronize a transfer of the plurality of data blocks between the microprocessor and the buffer memory.

17. The system-on-a-chip of claim 16, wherein the hardware-implemented logic block comprises:

a plurality of buffers configured to synchronize transfer of the plurality data block between the microprocessor transferring data at a first bit-width and the buffer memory transferring data at a second bit-width.

18. The system-on-a-chip of claim 16, wherein the hardware-implemented logic block comprises:

a plurality of buffers configured to synchronize transfer of the plurality of data blocks between the microprocessor transferring data at a first data rate and the buffer memory transferring data at a second data rate.

19. The system-on-a-chip of claim 8, wherein the memory controller further comprises:

a memory translator comprising:

a hardware-implemented logic block configured to synchronize a transfer of the plurality of data blocks between the buffer memory and the non-volatile semiconductor-based imperfect memory device.

20. The system-on-a-chip of claim 19, wherein the hardware-implemented logic block comprises:

a plurality of buffers configured to synchronize transfer of the plurality of data blocks between the microprocessor transferring data at a first bit-width and the buffer memory transferring data at a second bit-width.

21. The system-on-a-chip of claim 19, wherein the hardware-implemented logic block comprises:

a plurality of buffers configured to synchronize transfer of the plurality of data blocks between the microprocessor transferring data at a first data rate and the buffer memory transferring data at a second data rate.

22. The system-on-a-chip of claim 8, wherein the memory controller further comprises:

a memory interface configured to receive from the buffer manager the physical block address for the at least one data block, to provide the error correction code for the at least one data block, to write/read the at least one data block and associated error correction code to/from the non-volatile semiconductor-based imperfect memory device, and to provide the error correction/detection for the at least one data block using the at least one data block and associated error correction code read from the non-volatile semiconductor-based imperfect memory device.

23. The system-on-a-chip of claim 22, wherein the memory interface comprises a hardware implemented logic block.

24. A mobile electronic device comprising:

a system-on-a-chip comprising:

a microprocessor; and

a non-volatile semiconductor-based imperfect memory device; and

a memory controller configured to receive at least one data block from the microprocessor using an associated logical block address, to translate the associated logical block address to a corresponding physical block address, to provide for the at least one data block an error correction code (ECC) that is a function of the at least one data block, and to send the at least one data block and error correction code to the non-volatile semiconductor-based imperfect memory device using the physical block address.

21. The mobile electronic device of claim 20, wherein the non-volatile semiconductor-based imperfect memory device is an ultra-high density atomic resolution memory device.

22. The mobile electronic device of claim 20, wherein the non-volatile semiconductor-based imperfect memory device is a magnetic random access memory device.

23. A method of communicating data between a system-on-a-chip and a non-volatile semiconductor-based imperfect memory device, the method comprising:

locating on a same semiconductor a processor, a memory controller, and the non-volatile semiconductor-based imperfect memory device.